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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/643,276

08/18/2003

Chong H. Lee

174/212 Cont.

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06/01/2004

FISH & NEAVE

1251 AVENUE OF THE AMERICAS

50TH FLOOR

NEW YORK, NY 10020-1105

EXAMINER

LE, DON P

ART UNIT

PAPER NUMBER

2819

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/643,276

Applicant(s)

LEE ET AL.

Examiner

Don P Le

Art Unit

2819

*PL*

-- The MAILING DATE of this communication appears in the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9-16 is/are allowed.
- 6) ☐ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) 4-8 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 12/12/2003.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

*Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Raza et al. (US 6,510,487). Figure 2 of Raza discloses a programmable logic device, comprising:

Programmable logic circuitry (24');  
High speed serial interface circuitry (circuit providing data to 32), portions of which can be selectively be coupled to portions of the programmable logic circuitry;  
and

A plurality of channels of functional subcircuits (16', 18', 20', 22')) for selectively coupling portions of the programmable logic circuit and portions of the high speed serial interface circuitry.

3. Claims 2 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Kean et al. (US 5,737,235).

4. With respect to claim 2, figures 5-18 of Kean teach a programmable logic device, comprising:

Programmable logic circuitry (39);

Serial interface circuit for converting a serial data input signal to a plurality of parallel signals (see column 5, lines 1-25); and

Pattern detection circuitry for detecting byte boundaries of the parallel signals (see, figure 14, this is inherent in the circuit of Kean, otherwise Kean can not change serial data to parallel data, Kean must know when the data start and stop).

5. With respect to claim 3, it is inherent that there must be a circuitry to send parallel signals to other circuitry.

*Allowable Subject Matter*

6. Claims 9-16 are allowed.
7. Claims 4-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
8. The following is an examiner's statement of reasons for allowance:

With respect to claim 4, the prior art does not teach a circuitry for applying applies information between two adjacent byte boundaries.

With respect to claims 5 and 6, the prior art does not teach pattern detection circuitry is programmable with respect to what pattern is detected.

With respect to claim 7, the prior art does not teach circuitry for selectively applying information from the parallel signals to the programmable logic circuitry without regard for the bytes boundaries.

With respect to claim 9, the prior art does not teach channel alignment circuitry for synchronizing data in that serial interface circuit with data in a second of the serial interface circuits.

With respect to claim 13, the prior art does not teach a ten bit to eight bit decoder circuitry for converting information from ten bit of the parallel signals to eight further parallel signals.

With respect to claim 16, the prior art does not teach a rate matching circuitry.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P Le whose telephone number is 703-308-4890. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J Tokar can be reached on 703-305-3493. The fax

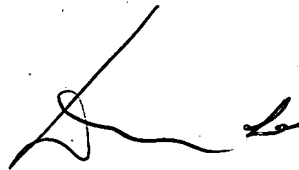
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phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/22/2004



**DONLE**  
**PRIMARY EXAMINER**